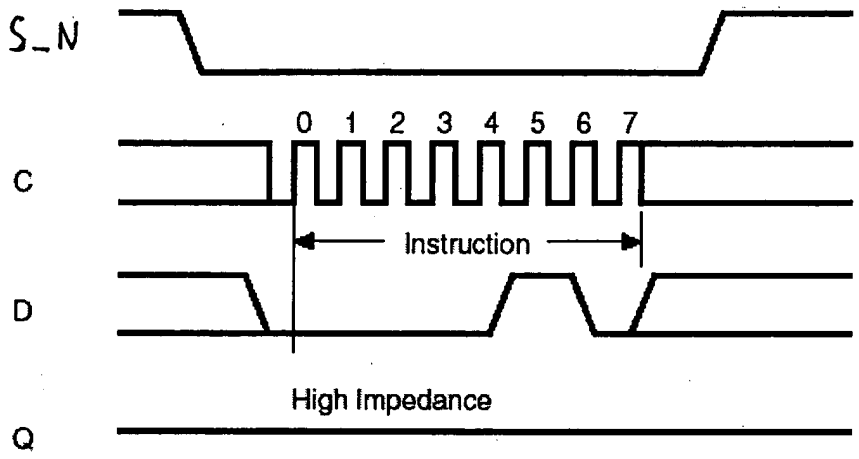
S_N
0 1 2 3 4 5 6 7
C
Instruction
D
High Impedance
Q

Fig.1

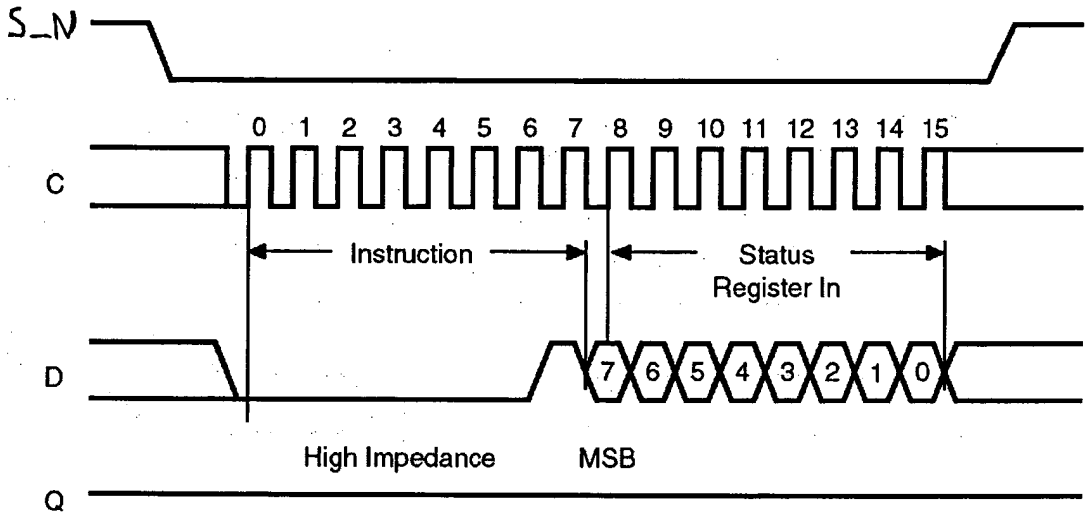
S_N
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
C
Instruction
Status
Register In
D
7 6 5 4 3 2 1 0
High Impedance
MSB
Q

Fig.2

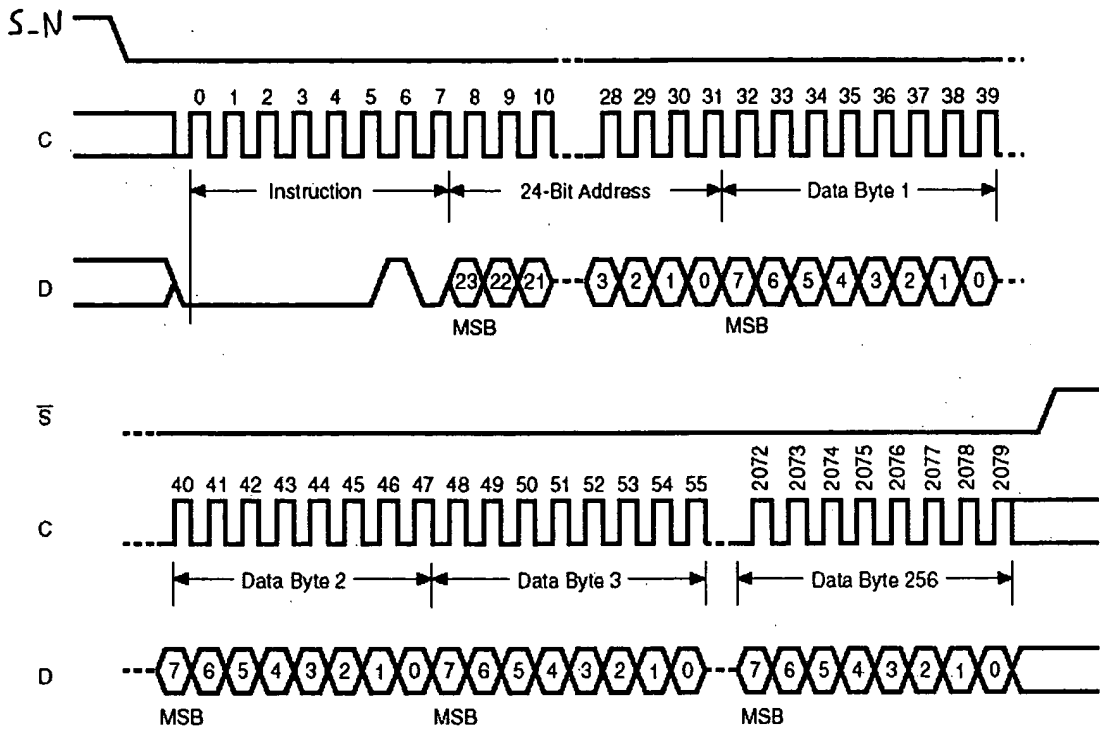
S_N
C
0 1 2 3 4 5 6 7 8 9 10 28 29 30 31 32 33 34 35 36 37 38 39
Instruction
24-Bit Address
Data Byte 1
D
23 22 21 3 2 1 0 7 6 5 4 3 2 1 0
MSB
MSB
S
C
40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 2072 2073 2074 2075 2076 2077 2078 2079
Data Byte 2
Data Byte 3
Data Byte 256
D
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
MSB
MSB
MSB

Fig.3

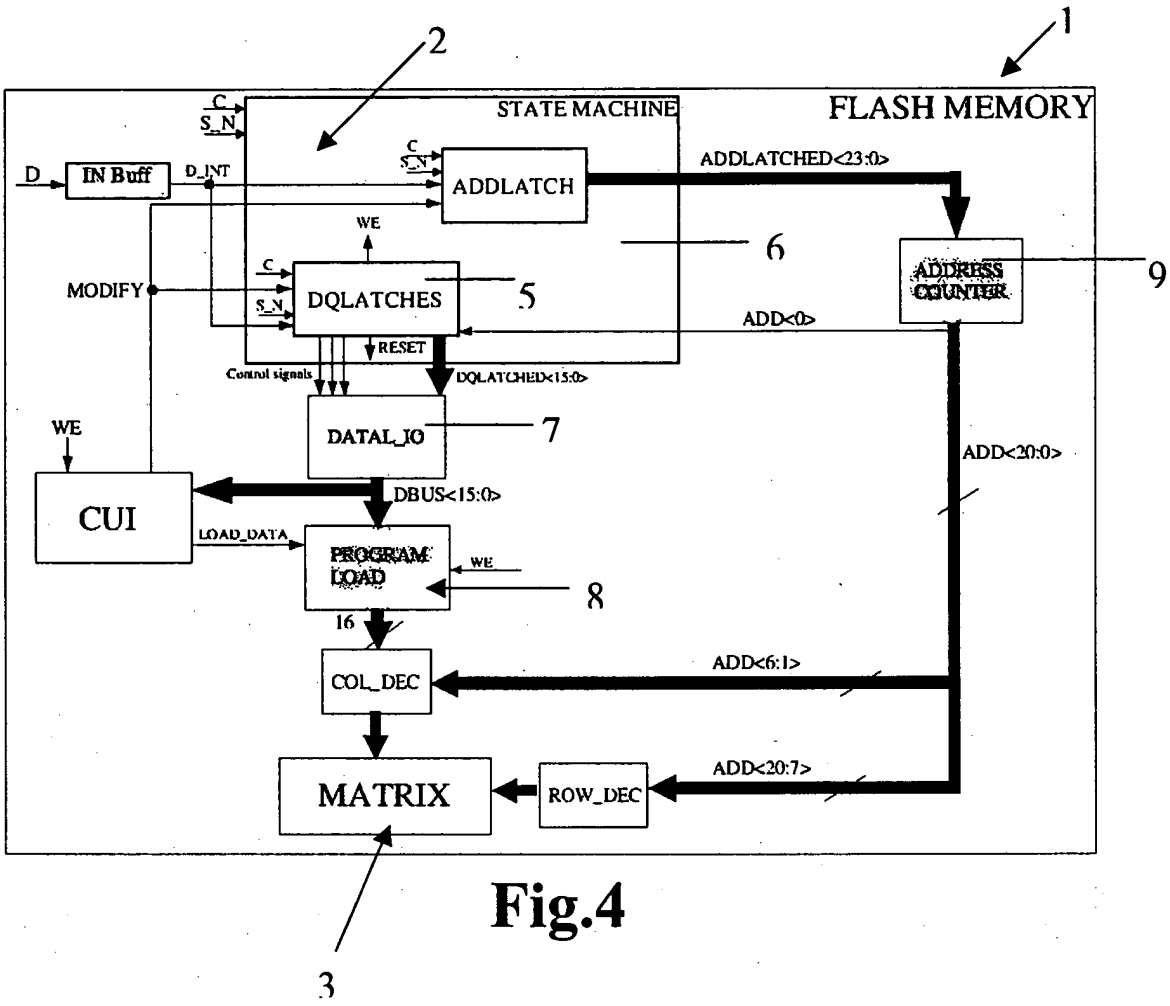
1
2
FLASH MEMORY
STATE MACHINE
C
S_N
D
IN Buff
D_INT
ADDLATCH
ADDLATCHED<23:0>
WE
6
ADDRESS COUNTER
9
MODIFY
DQLATCHES
5
ADD<0>
RESET
Control signals
DQLATCHED<15:0>
DATAL_IO
7
WE
ADD<20:0>
CUI
DBUS<15:0>
LOAD_DATA
PROGRAM LOAD
WE
8
16
COL_DEC
ADD<6:1>
MATRIX
ROW_DEC
ADD<20:7>
3

Fig.4

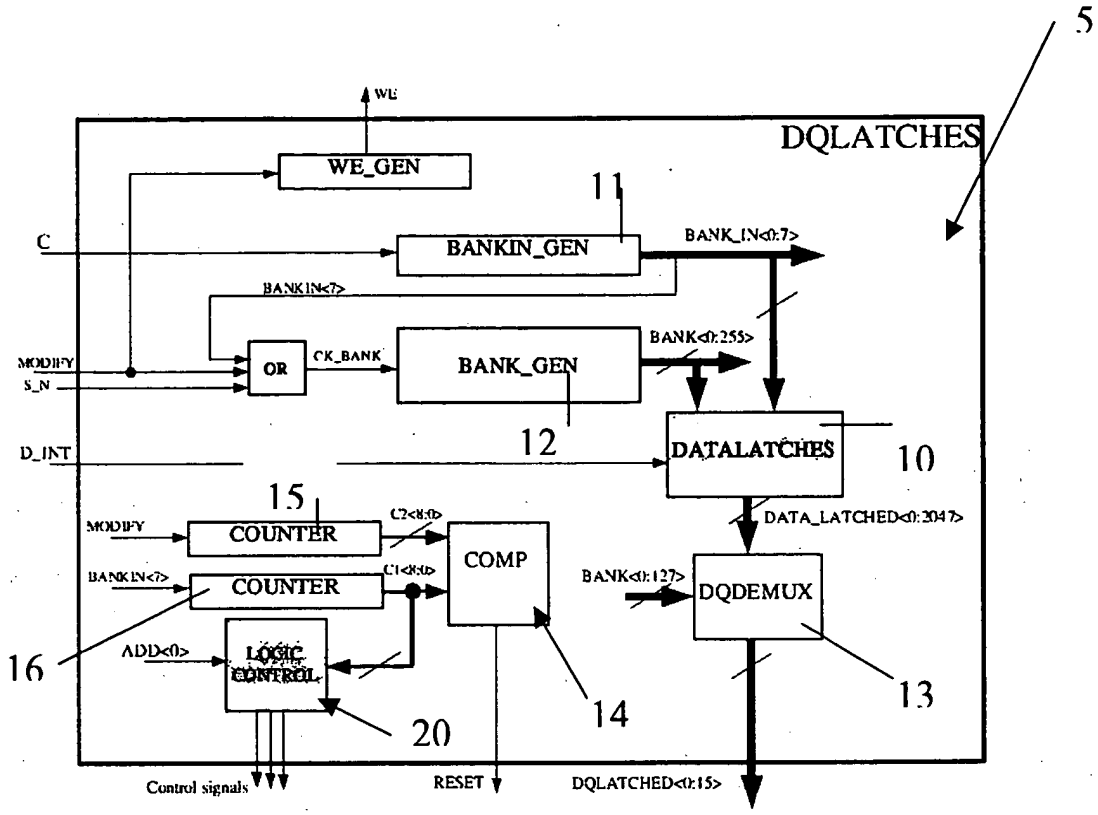
5
DQLATCHES
WE
WE_GEN
11
C
BANKIN_GEN
BANK_IN<0:7>
BANKIN<7>
MODIFY
S_N
OR
CK_BANK
BANK_GEN
BANK<0:255>
12
D_INT
DATALATCHES
10
15
MODIFY
COUNTER
C2<8:0>
COMP
DATA_LATCHED<0:2047>
BANKIN<7>
COUNTER
C1<8:0>
BANK<0:127>
DQDEMUX
16
ADD<0>
LOGIC CONTROL
20
14
13
Control signals
RESET
DQLATCHED<0:15>

Fig.5

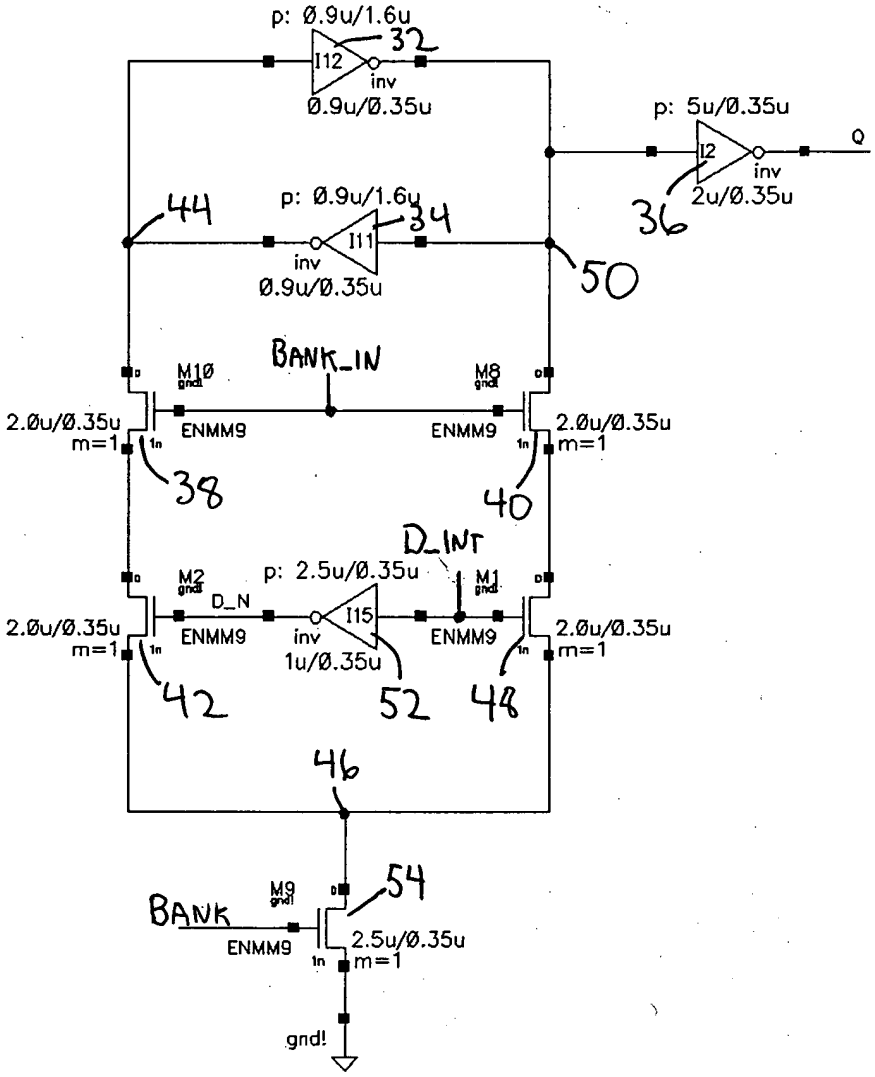
p: Ø.9u/1.6u
32
I12
inv
Ø.9u/Ø.35u
p: 5u/Ø.35u
Q
I2
inv
2u/Ø.35u
36
44
p: Ø.9u/1.6u
34
I11
inv
Ø.9u/Ø.35u
50
BANK_IN
M10
M8
2.Øu/Ø.35u
m=1
ENMM9
ENMM9
2.Øu/Ø.35u
m=1
38
40
D_INT
M2
p: 2.5u/Ø.35u
M1
D_N
2.Øu/Ø.35u
m=1
ENMM9
I15
inv
1u/Ø.35u
ENMM9
2.Øu/Ø.35u
m=1
42
52
48
46
M9
54
BANK
ENMM9
2.5u/Ø.35u
m=1
gnd!

Fig.6

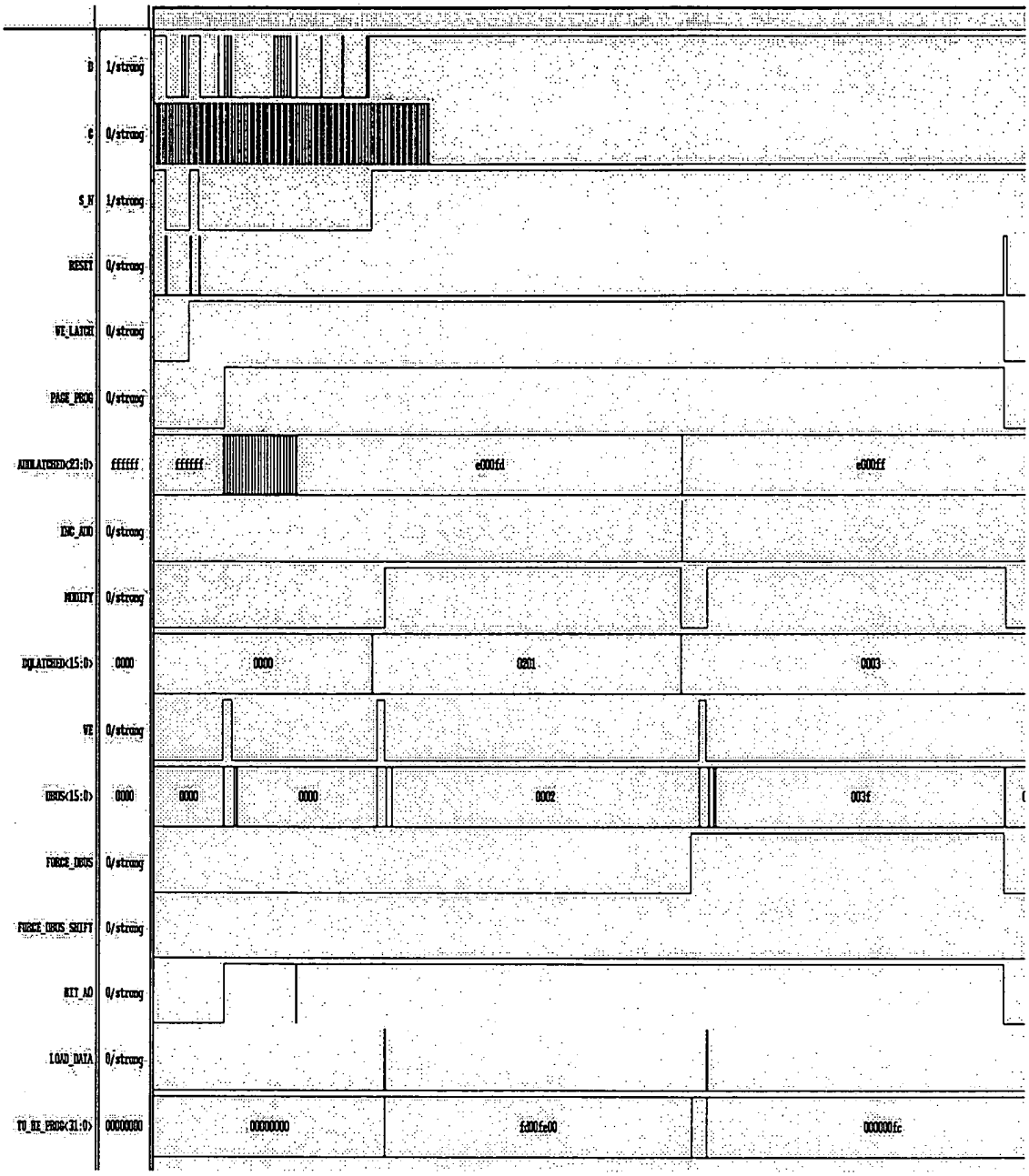
D
C
S_H
RESET
WE_LATCH
PAGE_PROG
ADDLATCHED<23:0>
INC_ADD
MODIFY
DQLATCHED<15:0>
WE
DBUS<15:0>
FORCE_DBUS
FORCE_DBUS_SHIFT
RET_AD
LOAD_DATA
TO_BE_PROG<31:0>
1/strong
0/strong
ffffff
e001fd
e000ff
0000
0201
0003
0002
003f
00000000
fc001fc00
000000fc

Fig.7

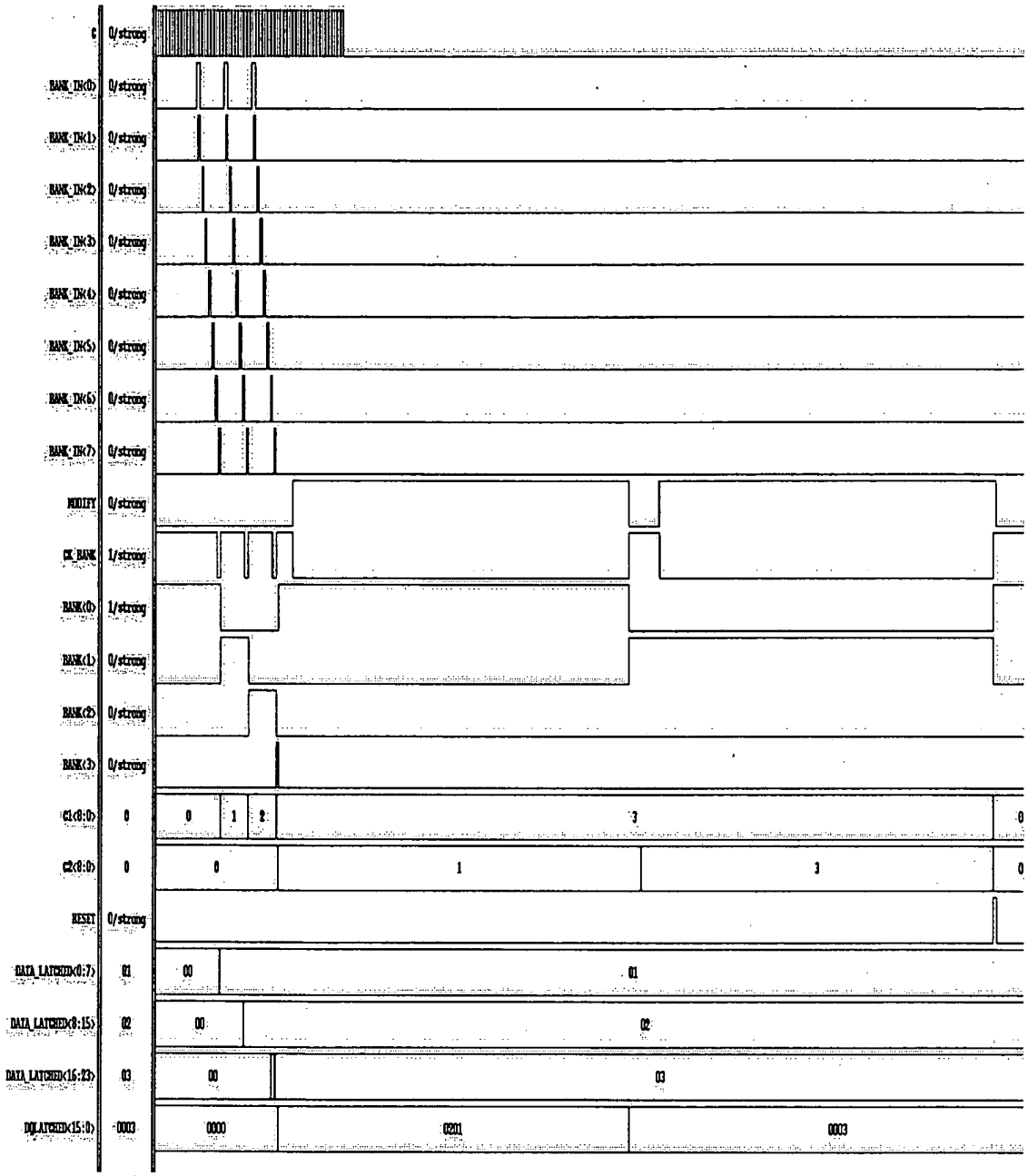
C
BANK_IN<0>
BANK_IN<1>
BANK_IN<2>
BANK_IN<3>
BANK_IN<4>
BANK_IN<5>
BANK_IN<6>
BANK_IN<7>
MODIFY
CK_BANK
BANK<0>
BANK<1>
BANK<2>
BANK<3>
C1<8:0>
C2<8:0>
RESET
DATA_LATCHED<0:7>
DATA_LATCHED<8:15>
DATA_LATCHED<16:23>
DQ_LATCHED<15:0>
0/strong
1/strong
0
1
2
3
00
01
02
03
0000
0201
0003

Fig.8

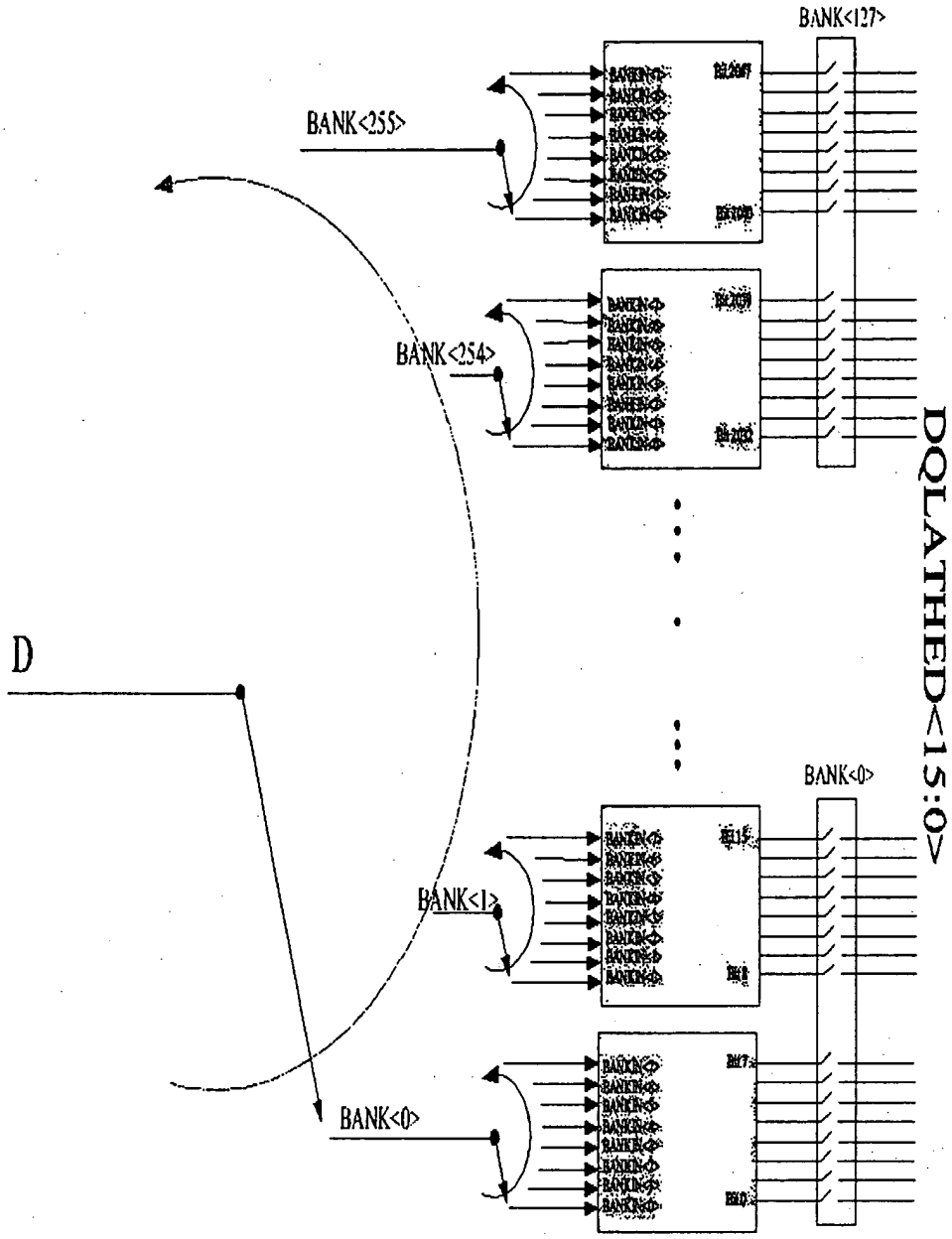

Fig.9